





Research and Development Technical Report

ECOM - 4493

TRANSIENT WAVEFORM ANALYSIS OF SWITCHING CONVERTER

Emil Kittl

Electronics Technology & Devices Laboratory

April 1977

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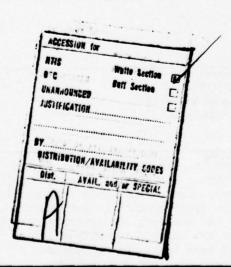
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Item 20. ABSTRACT -Continued

Adapted to a PDP-8/I Minicomputer operating in TSS/8 Time Sharing Mode, a X-Y Digital Plotter (HP 7200A) is used to plot the transient waveforms. In the analysis, four normalized state variables of the converter circuit have been used which are defined as the ratios of time dependent quantities for the capacitor voltage, inductor voltage, primary transformer voltage, and current with respect to the DC input voltage. Variation of the diode conduction time intervals is used as independent switch modulation parameter and its value is normalized with respect to the period of the circuit resonance frequency OMEGA = 1/Square-Root (L·C). Results of the transient analysis study are presented as ratios of maximum electrical stresses for the selected state variables. The relationship of circuit component parameters to transient stresses are discussed with respect to variation of the control parameter representing the switch modulation time.

The inherent fast response of the specific resonance converter circuit to switch modulation control provides simple interpretation of the control concept with respect to critical transient stress behavior.

The fundamental relationship of the discrete switching time periods to operational changes of input and output voltages is analyzed for steady state condition and provides a suitable basis for feedback control loop design.



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TRANSIENT WAVEFORM ANALYSIS OF SWITCHING CONVERTER

Transient Studies for a Series-Resonance
DC to DC Converter Using Anti-Parallel Diodes
and Controlled Transistor Switching Time (Computer Study)

INTRODUCTION

Advanced military power processing technology is guided by three significant objectives: 1. Reduction in weight and size of power processors which are necessary links between generators of raw electrical power and sophisticated user mission equipment; 2. Improvement in efficiency through reduction in operating losses which is an important key to thermal design consideration and component packaging density, indirectly affecting size and weight; 3. Component and operational reliability as expressed in mean time before failure (MTBF).

The present trend in this technology clearly indicates emphasis on advanced switching technology using semiconductor devices as the prime power processors. This concept permits digitized power flow control between input and output terminals with the inherent advantage of faster control response, better waveform resolution, and smaller transformers, inductors, and filters. All of these advantages are directly related to the capability of handling higher switching frequencies. In this respect, present limitations are identified by: 1. The inverse relationship between power handling capability and switching time of power transistors, rectifiers, and silicon controlled rectifiers (SCR), and 2. The interrelation between circuit configuration of the power processor and maximum steady state and transient stresses experienced in its critical components.

While the area of improved semiconductor power switching components is of great concern and the need for faster switching transistors with higher power handling capability is well recognized, it is the power switching circuit concept and its impact on technology advancement that will be focused on in this report.

This study is limited to an analysis of a DC to DC converter configuration. The most significant design parameter of such a converter is the ratio of input and output voltages and their operational variation. There are two components of this ratio which are of importance and should be distinguished: 1. The scaling factor, which is defined as the ratio of the average input voltage to average output voltage, and 2. The control ratio range, which is defined as maximum input voltage over minimum output voltage versus minimum input voltage over maximum output voltage.

With the exception of extreme input/output voltage ratios, scaling is not a significant design problem in the DC to DC converter and because of the usual requirement for complete input to output isolation, it is achieved by a transformer as the representative circuit element. It is the range of the control ratio which defines the sophistication of a DC to DC converter circuit. The concept of digital power flow within discrete time elements requires that a variable slug of input energy be processed through the

power transfer circuit such that it meets the average output power requirements. From this discussion, it is obvious that the range of change in discrete processing time is directly proportional to the previously defined control ratio range. In turn, the need for storage capability in the filter sections (input and output) is also proportional to this range of discrete processing time which is directly reflected in the size and weight of power processing circuit components and filters. At a first glance, the nature of DC input and output requirements would make it ideal to process discrete time energy slugs with rectangular pulse current and voltage wave shapes (pulse width modulation). However, achievable dv/dt and di/dt parameters directly depend on switching component capability and circuit design. Therefore, with the desired increase in switching frequency, it is realized that the concessions that have to be made in deviating from ideal rectangular pulse waveforms become so severe that this idealization is no longer a useful concept. Consequently, a new concept approach follows logically. If idealized rectangular wave shapes can not be processed, then it may be feasible to go to sinusoidal wave shapes which are ingredients of idealized resonance circuits. This concept has been widely explored on an empirical basis in the past five years and with remarkable success. One of the most salient features of this approach is the use of zero current switching without the need of forced commutation, which considerably simplifies and reduces circuit requirements and increases the power handling rating of the switching components. This in turn allows one to go to higher switching frequencies which more than compensates for the increased rating of energy storage components that is related to the difference between sinusoidal and rectangular wave shapes.

The series resonance converter circuitry selected for analysis in this report represents one of the simplest circuit configurations of a DC to DC switching converter with a minimum of components in the power processing circuit. It is true, that the deviation from the ideal digitized energy flow concept with rectangular wave shapes presents a more complex problem to the analysis of power transfer in this circuit. This has generated the need for a more detailed transient waveform analysis and a better understanding of the control concept that relates discrete time control to the significant output performance parameters in the resonance type converter.

ANALYSIS

The analysis applies to the series resonance DC to DC converter circuit, as shown in Figure 1, which has been treated in some detail in the literature.² The input symmetry of the circuit, with respect to the split resonance capacitors Cl and C2 and the two transistor switching elements TRl and TR2, permits simplifications in the equivalent power transfer circuits which are applicable for the 4-cycle consecutive switching states as shown in Figure 2. It is seen that these circuits all contain the same elements

F. C. Schwarz, "Engineering Information on an Analog Signal to Discrete Time Interval Converter (ASDTIC)," NASA CR-134544 Report, Contract NAS 3-16791 (NASA), Power Electronics Associates, June 1974.

²F. C. Schwarz, "An Improved Method of Resonant Current Pulse Modulation for Power Converters," Proc. IEEE Power Electronics Specialists Conference, PESC '75 Record, pp. 194-204 (1975).

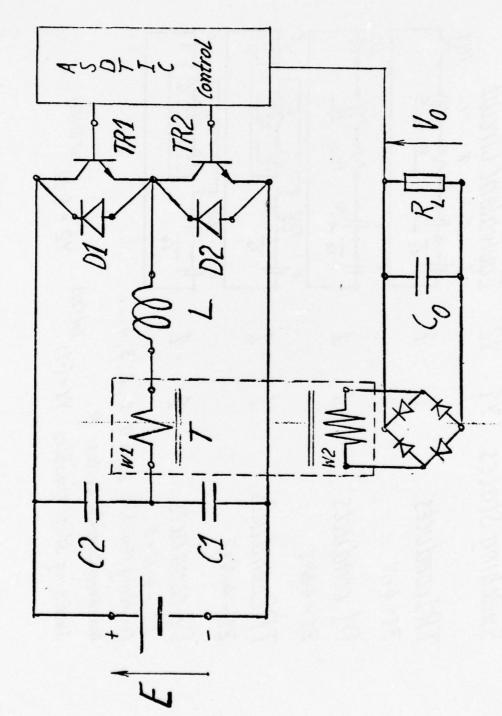


Figure 1. Power Switching Circuit for Series-Resonance DC/DC-Converter

Equivalent Circuit	TR1 conducts 1 1 Hook over 1	10 - 10 - 1 - 22 - 1 - 21 - 22 - 1 - 21 - 2	Hoope Months H	The Warden of the		$1) Y2 = (-1)^{2nt}(E1/2)$
72	7	7		1-1	3,4	.1) Int (23
77	7	1 1-	7-1	7	0,1,2, N)=1/
Switching States	TR1 conducts 21= 4.N	D1 conducts	TR2conducts	D2 conducts	Counting Variable: Z1 = 0,1,2,3,4 Number of Converter Cycles: N	Switching State Variables Y1=(-1) Int (21)

Figure 2. Switching States and Equivalent Circuits

if Cl = C2; TRl and TR2 are considered as equivalent, idealized switches. The transformer coupling of the output loop containing a single filter capacitor (see Figure 1) is represented in Figure 2 by the impressed voltage V_T on the primary winding of this ideal transformer. The switching states are characterized by their respective sets of boundary conditions at the beginning of each switching period. These boundary conditions directly follow from the end of period state of the preceding switching cycle. Therefore, the solution in the time domain for any of the selected voltages and currents, which have been considered in the state equations of the circuit, represent a continuous wave train which is an exact replica of waveforms that may be examined experimentally on a scope, using a converter circuit for which Figure 1 is a representative model.

A computer program has been written that calculates and plots out, on a X-Y recorder, the time domain solutions of each state variable as a continuous string of waveforms. This allows evaluation of transient stresses and steady state conditions. Step function changes of operational conditions can be introduced as a new set of input parameters which affect the boundary conditions at each beginning of a switching state. This allows studying of transient and stability problems and even permits control loop design evaluations on the basis of Analog Signal to Discrete Time Interval Converter (ASDTIC) type control functions.³

The termination of each transistor conduction period is based on a test criterion of zero current flow. Then the analysis of the next diode conduction period is executed by the computer for the predetermined diode conduction time which is introduced as a dimensionless parameter relating diode conduction time to the half-period time at resonance frequency. Calculated output parameters are also dimensionless and normalized with respect to the input voltage. The chosen range of the normalized diode conduction time is zero to unity (0 < 22 < 1). This avoids interruptions of power flow in the input circuit for normal load conditions. Results of the analysis are presented for a converter circuit configuration which operates over a frequency range from 13.5 to 27 kHz. For the specified range of diode conduction period of (0 < 22 < 1), a range of the output to input voltage control ratio (V_0/E) of 2.5 to 0.5 can be utilized at nominal load.

ASSUMPTIONS AND CONSTRAINTS

The simplifying assumptions which have been selected for the analysis are:

- l. All passive circuit components are represented by lumped parameters of L, C, and R.
 - 2. Inductors and capacitors are considered ideal and lossless.

³F. C. Schwarz, NASA CR-134544 Report, op. cit., p. 2.

- 3. The coupling transformer is considered an ideal voltage scaling device, without losses and represented by a turns ratio M = W_1/W_2 .
- 4. Transistors and diodes are considered lossless, instantaneous switches characterized by the two states on and off. They are unipolar conducting devices requiring the ending of a discrete switching period whenever the current reaches zero. This requirement determines the four equivalent circuit configurations shown in Figure 2.
- 5. The switching effect of the rectifier bridge in the DC output circuit is modeled by a function V_T = Sign (I_L) M V_O , implied by the change of sign of V_T whenever the current changes direction.
- 6. Continuity of capacitor voltages and inductor currents is a requirement for time boundary conditions between switching states.

STATE-VARIABLES

In each of the four switching states, the circuit state can be described by three selected state variables. To facilitate a dimensionless analysis, the state variables selected are $V_{\rm C}/E$, $V_{\rm L}/E$, and $V_{\rm T}/E$. Two other variables important for circuit evaluation are J/E, the normalized value of the inductor current, and $V_{\rm C}/E$ the normalized value of the DC output voltage. Both are derived by simple relations with $V_{\rm C}$ and $V_{\rm T}$, respectively, and were not treated as independent variables, in order to keep the coefficient matrix to a simple manageable 3 by 4 matrix.

General Expressions for the State Equations in S-Space

$$V_{y, x}(S) = \frac{A_{yx1}}{S_0} + \frac{A_{yx2}}{S - S_{x1}} + \frac{A_{yx3} \cdot S + A_{yx4}}{(S - S_{x2})^2 + S_{x3}^2}$$
 (1)

where

y subscript defines the state variable (Y = 1 to 3)

 $x \cdot \cdot \cdot \cdot$ subscript defines the order of the system (x = 0 to 3)

The characteristic equation in S-Space is:

$$s^{14} + B_{1}s^{3} + B_{2}s^{2} + B_{3}s = 0 (2)$$

The roots of Equation (2) are only a function of the circuit element parameters C, L, R_L , C_O , and M. The values A_{yx} in Equation (1) depend on the initial boundary conditions for each switching state and are expressed by matrix equations of the form.

$$A_{yx} = Qs_{x,y} \cdot E_{y}(x_{0})$$
 (3)

The matrix Qs , has elements which are only functions of S_{xi} , while $E_y(x_0)$ is a linear vector representing boundary conditions between the four switching states.

Solution in the Time Domain for the State Variables

$$V_{\mathbf{y}}(t) = X_{\mathbf{y},0} \cdot \exp(S_{\mathbf{x}0} \cdot t) + X_{\mathbf{y},2} \cdot \exp(S_{\mathbf{x}1} \cdot t) + X_{\mathbf{y},3} \cdot \exp(S_{\mathbf{x},2} \cdot t) \cdot \sin(S_{\mathbf{x},3} \cdot t + \mathbf{a}_{\mathbf{y}})$$
(4)

with

$$\mathbf{a}_{y} = \text{Arct } (S_{x,3}/(S_{x,2} + X_{y,3}/X_{y,2}))$$
 (5)

The subscript y in Equations (4) and (5) defines the state variable and the coefficients X_{yx} are derived from A_{yx} . The complete circuit analysis is presented in Appendix A and the computer program for calculating the time domain solutions is presented in Appendix B.

APPLICATION OF ANALYSIS

Steady State Conditions

The solution of the steady state condition requires the cyclic periodicity of the voltage waveforms as described by Equation (4). As shown in Figure 2, the sequence of the four switching periods is fixed. At the end of the fourth switching period, the system must return to the values at the beginning of the first switching period. The mathematical expression for this condition requires solution of a set of transcendental equations. complexity of these equations does not permit an explicit solution in the form of Equation (4) by defining the values of X_{VX} for steady state as a function of the circuit parameters. The criterion for the existence of a stable, steady state solution can, however, be tested directly by execution of the computer program for any given set of circuit input parameters C, Co, L, RL, and M. A set of initial boundary conditions must be chosen for the start. If after a reasonable length of time, transient conditions cease and the computer output shows a stable cyclic wave train, the stable steady state condition can be directly read from the specific features of this wave train. The criterion for a single valued, steady state condition which is correlated with a set of imput circuit parameters is given by the condition that the steady state waveform is independent of the initial boundary conditions selected.

Mode 1, Continuous Inductor Current Mode

An example of the evaluation of a steady state condition for a given set of circuit parameters and a chosen constant value Z2 of the discrete diode conduction time is shown in Figures 3 to 5. Figure 3 shows the first six cycles after initial start-up condition with circuit input parameters (C, C_0 , L, M) and operational parameters (R_L , Z2) indicated. The wave shapes for the normalized values of voltage V_C on the series capacitor, the voltage V_L on the inductor, and the current J through the inductor are plotted together with voltage V_T on the primary winding of the transformer.

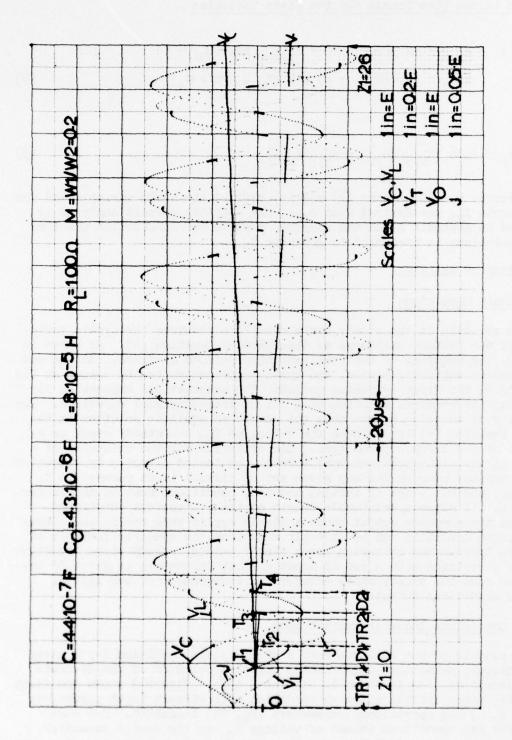


Figure 3. Start-Up Transient Wave Shapes for Z2=0.5, Z1=0-26

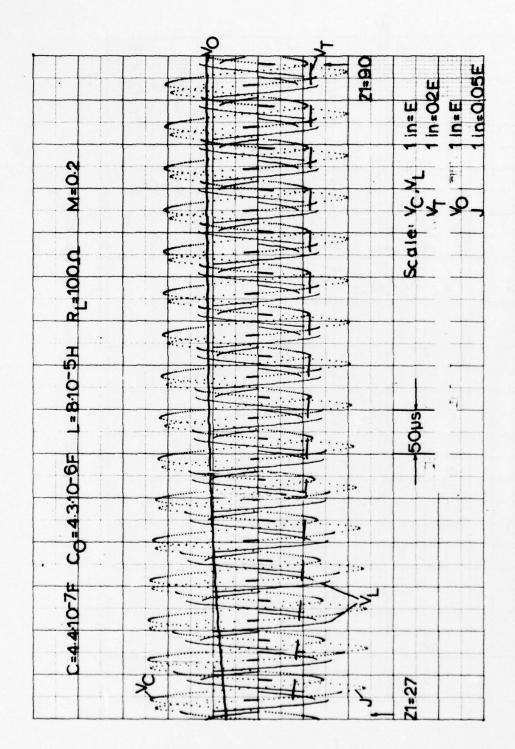


Figure 4. Transfent Wave Shapes for Z2=0.5 and Z1=27-90

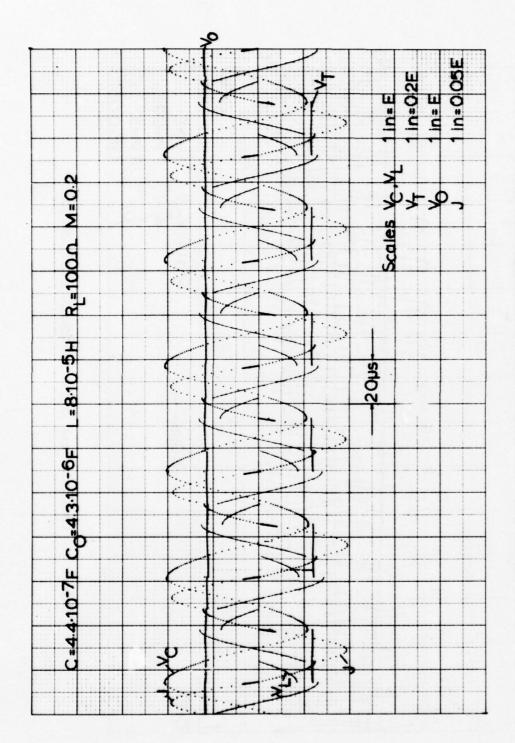


Figure 5. Transient Wave Shapes for Z2=0.5 and Z1=300-324

Also plotted is the DC-output voltage V_{O} . The scale factors for V_{T} and V_{O} have been chosen such that their ratio is identical with the winding ratio M on the transformer. It is seen that V_{T} is identical with the trace of V_O in the positive half-cycle of J and $V_T = -M \cdot V_O$ in the negative half cycle. Negative values of V_{T} are associated with negative values of J. The initial set of boundary conditions chosen for the beginning of the first conduction period of transistor TR1 are: $V_{C1} = V_{C2} = E/2$, J = 0, $V_T = 0$. This means that the input voltage is equally divided among the 2 series capacitors Cl and C2 (see Figure 1). When transistor TR1 is turned on at point To, the output filter capacitor Co is in a discharged condition so that $V_{T}(0) = 0$. The current J charges capacitor Cl, while capacitor C2 is being discharged. Curve VC2 is not shown on the plot but is antisymmetric to VC1 with respect to a line drawn parallel to the time axis with the value E/2. The current J is almost sinusoidal, reaches a maximum, and then swings toward zero. Note that the plotted interval of points has been reduced by a factor of 10 as the current approaches zero. This measure provides higher accuracy for the time limitation criterion of the first transistor conduction period which ends when J reaches zero. The normalized inductor voltage $V_{\rm L}/E$ starts with a value of 0.5 and swings to a negative value of approximately -0.5 at the end of the first transistor conduction period (point T1). The voltages V_T and V_O increase very slowly, due to the fact that the output filter capacitor is about 10 times larger than the resonance capacitor and its equivalent value reflected into the primary circuit is increased by the factor $1/M^2 = 25$. This relationship, which has been selected to reduce the ripple voltage in the output, is very important for understanding the nature of start-up transient wave shapes during the first few cycles which show insignificant dependence on the value of the load resistance R_{I.}. The conduction period of diode DL begins, at point Tl, with a negative rising current J and ends when this current reaches its maximum value at T2 after a time equivalent to Z2 = 0.5. The inductor voltage is seen as swinging back to zero and $m V_{Cl}/E$ approaches 1. At the beginning of the diode conduction, V_T jumps to a negative value and keeps rising in absolute value. At point T2, transistor TR2 is turned on. Consulting the equivalent circuit in Figure 2, we have a situation where C2 is discharged (because $V_{C1} \approx E$) and since V_{TP} is still very small, the bulk of the input voltage E appears on the inductor as a negative voltage $V_{\rm r}/E = -1$ as can be seen in the graph. During the TR2 conduction period, $V_{
m L}^{
m L}$ approaching zero causes a further increase of the current in the negative direction. Capacitor C2 is rapidly charged by this current to a positive value, while capacitor Cl discharges. When the current reaches its negative maximum, V_{Cl} and V_{L} are approximately 0 and $V_{C2} \approx E$. As the current swings back to zero, V_{C2} rises further and reaches a value of approximately $V_{C2} \approx 2E$ at the end of the conduction period of transistor TR2 at point T3. Since V_{C2} is not shown on the computer graph, Figure 3, its value is inferred from the condition $V_{\rm C2}$ = E - $V_{\rm C1}$. With $V_{\rm C1}$ \approx -1.1 E, $V_{\rm C2}$ = 2.1 E. When conduction through transistor TR2 ceases at point T3, diode D2 starts conducting the now positive current for a period equivalent to Z2. Note the sharp rise of the diode current to its maximum value at the start of this period which is caused by a rapid discharge of capacitor C2 from the value of 2.1E to approximately 1.1E. At point T4, transistor TR1 is turned on again and the first cycle is completed. Note that the state of the circuit has now significantly changed as compared to the initial boundary conditions at point To. Capacitor Cl shows a slight negative

charge $V_{\rm Cl}$ = -0.1E. The initial current of the next transistor conduction starts with an appreciable positive value (J = +0.084 E) and, therefore, reaches a much higher maximum value. The process of buildup of stored energy in the capacitor and inductor continues until about the end of cycle 3 (Zl = 12) where $V_{\rm C}$ reaches a maximum value of +2.62E. At this point, $V_{\rm O}$ has reached a value of 0.386E and the energy dissipation in the load resistor ((0.38 E)2/100) is no longer negligible. The trend in the following cycles is now reversed, more stored transient energy is transferred to the load and dissipated. Peak currents and voltages begin to fall. Figure 4 shows a larger portion of the continuing wave train compressed into the time scale. It is seen that after about 25 cycles a steady state condition is approached, which can be best judged by the slow rising value of $V_{\rm O}$. Figure 5 shows enlarged values of cycles Zl = 300-324 from which the following results of the steady state condition are deduced:

$$Z2 = 0.5$$
; $R_L = 100 \Omega$; $Z1 = 320$
 $T_{1/2} = 23.77 \mu s$; $f = 21.03 \text{ kHz}$
 $J_{\text{max}} / E = 0.096$; $J_{\text{av}} / E = 0.058$; $J_{\text{max}} / J_{\text{av}} = 1.644$
 $V_{\text{Cmax}} / E = 2.07$; $V_{\text{Cpp}} / E = 3.14$
 $V_{\text{Tav}} / E = 0.201$; $V_{\text{O}} / E = 1.005$

A second case for a larger diode conduction period Z2 = 0.75 is shown in Figures 6 and 7. It is seen from Figure 6 that the initial transient maxima for V_C and J are now much smaller than those for Z2 = 0.5. Figure 7 shows the waveforms under steady state conditions for Z1 = 100 - 120 with the following results:

$$Z2 = 0.75$$
; $R_L = 100 \Omega$; $Z1 = 120$
 $T_{1/2} = 29.4 \mu s$; $f = 16.99 \text{ kHz}$
 $J_{\text{max}}/E = 0.058$; $J_{\text{av}}/E = 0.034$; $J_{\text{max}}/J_{\text{av}} = 1.663$
 $V_{\text{Cmax}}/E = 1.645$; $V_{\text{Cpp}}/E = 2.29$
 $V_{\text{Tav}}/E = 0.139$; $V_{\text{O}}/E = 0.695$

A similar computer plot is shown for Z2 = 0.875, Z1 = 0 to 16 in Figure 8. Comparing Figures 3, 6, and 8 it is seen that the start-up transients diminish when Z2 increases. Steady state condition is reached after about 25 cycles. Figure 9 shows the wave shapes for this condition and indicates the following parameters:

Z2 = 0.875;
$$R_L$$
 = 100 Ω ; Z1 = 104

 $T_{1/2}$ = 32.905 μ s; f = 15.195 kHz

 J_{max}/E = 0.0486; J_{av}/E = 0.0279; J_{max}/J_{av} = 1.740

 V_{Cmax}/E = 1.5443; V_{Cpp}/E = 2.0886

 V_{Tav}/E = 0.1124; V_{O}/E = 0.5623

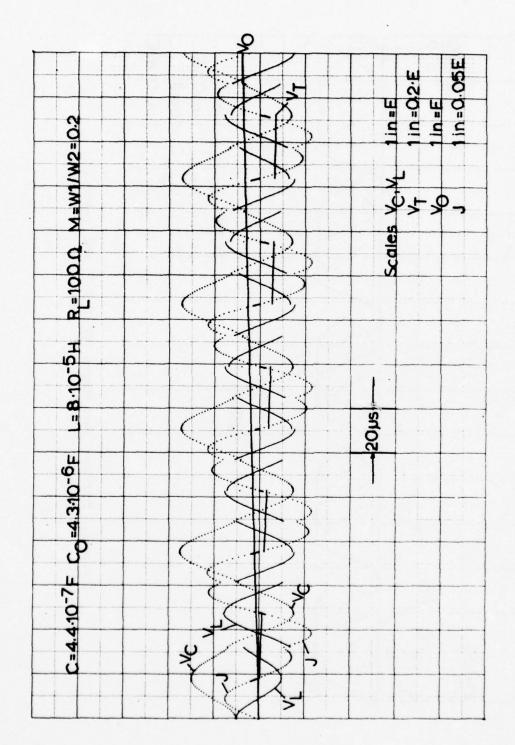


Figure 6. Start-Up Transient Wave Shapes for Z2=0.75 and Z1=0-20

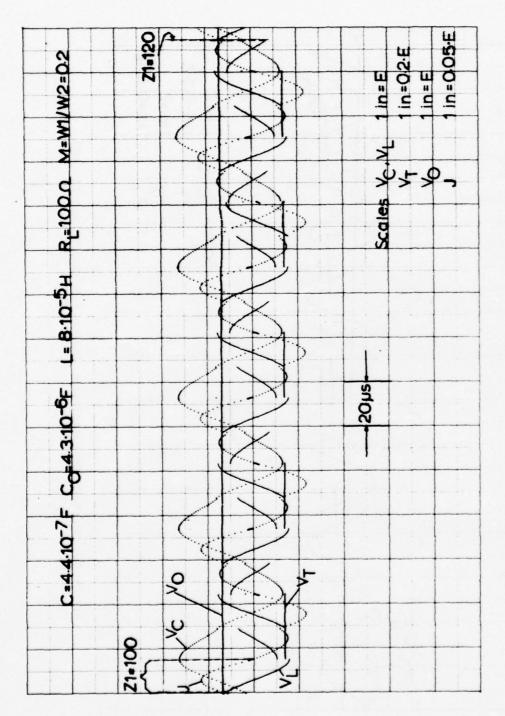


Figure 7. Transient Wave Shapes for Z2=0.75 and Z1=100-120

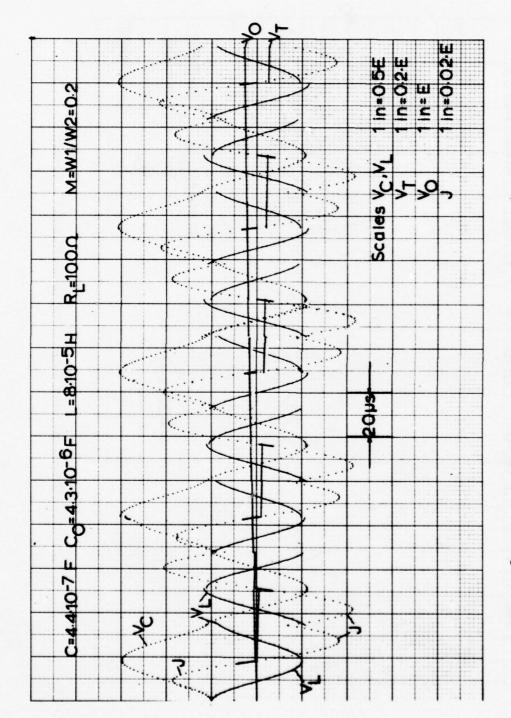


Figure 8. Start-Up Transfent Wave Shapes for Z2=0.875 and Z1=0-17

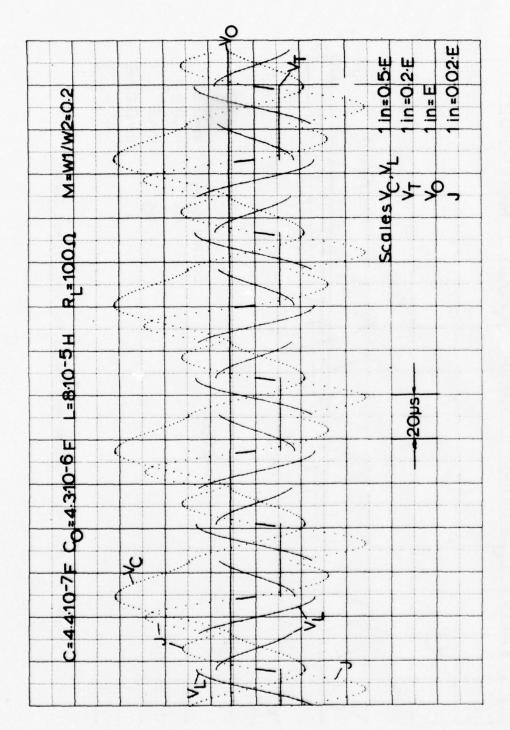


Figure 9. Transient Wave Shapes for Z1=0.875 and Z1=90-107

Similar computer plots were obtained for values of Z2 = 0, 0.25, 0.375, and 1. A summary of these results is presented in Table 1 and as a graph in Figure 10. These results are for a single value of load resistance ($R_{\rm L}$ = 100 Ω) which was considered nominal load. The curve labeled $V_{\rm O}/E$ in Figure 10 clearly shows the range of voltage control $V_{\rm O}/E$ to be 2.5 to 0.5 for a range of dwell time 0< Z2<1. It is also seen that the maximum capacitor voltage increases approximately by a factor 2 over this range, while the ratio $J_{\rm m}/J_{\rm av}$ varies only slowly with Z2. In contrast, the maximum transient current to steady state average current ratio shows a drastic increase as Z2 decreases to zero (see curve labeled $J_{\rm Tm}/J_{\rm av}$). This behavior raises interesting questions on the dynamic response of this converter and on the question of how to design a control system which avoids excessive component stresses. While the basic tools for such a study are provided in this report, the study of control concepts and design optimization is beyond the scope of this report.

Mode 2, Zero Diode Current Mode

As can be seen from Figure 2 (Case 2 and Case 4), whenever $E + V_T > V_C$, the diode (Dl or D2) is negatively biased and current cannot flow in the Inductor L. This condition occurs particularly at low load and the condition occurs particularly at load and the condition occurs initial start-up transient condition. Figure 11 shows a computer graph indicating a step change in the load value from the nominal $R_{L} = 100$ M to $R_{\rm T}$ = 1000 Ω at the end of switch period Z1 = 210. All other parameters are the same as for Figure 9 with the exception of the time scale. Immediately after this step change of $R_{\rm L}$, the transformer voltage $V_{\rm T}/E$ and the output voltage $V_{\rm O}/E$ start to rise. During the diode conduction period, the peak current value of J/E gradually decreases, while at the same time, each succeeding peak value of J/E in the transistor conduction period rises. Figure 12 shows a continuation of the graph of Figure 11. At z1 = 346, at the end of the TR2 conduction period, $1 + V_{m}/E$ exceeds the capacitor voltage V_C/E and Diode D2 is reverse biased at the beginning of Z1 = 347. This means that the diode current is zero. The transistor peak current has reached its maximum at Zl = 346 and begins to fall in the succeeding switch periods. Since the average value of the transistor current is still larger than the equivalent load current through RL, the output filter capacitor Co still receives an appreciable charging current during the transistor conduction period and, as a result, the values V / E and V / E continue to increase. The rapid feedback between transistor current and voltage on the resonance capacitor is seen between switching cycles Z1 = 346 to Z1 = 378. At the next transistor switching period (Z1 = 382), the transistor is reverse biased by the condition $1 + V_C/E < V_m/E$ and cannot conduct. A new mode, Mode 3, starts.

Mode 3, Zero Transistor, Zero Diode Current Mode

This mode continues and is characterized by an effective decoupling of the primary input and secondary output stage. It can only be changed by the slow decay of the voltage on the filter capacitor $V_{\rm O}$ through discharge into the load resistor $R_{\rm L}$. Therefore, it is clearly seen that a low load current (high value of $R_{\rm L}$) will prolong this mode. The continued wave train, shown in Figure 13, indicates that at Z1 = 398 a small transistor current again starts to flow when $V_{\rm T}/E$ has reduced to a value of 0.5.

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Table 1. Summary of Normalized Transient and Steady-State Parameters

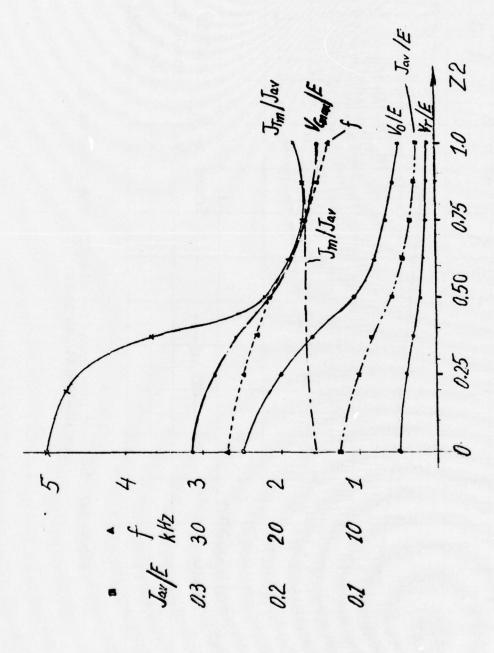


Figure 10. Normalized Steady State Parameters Versus Diode Conduction Time

Z2=T2/(T · V L · C)

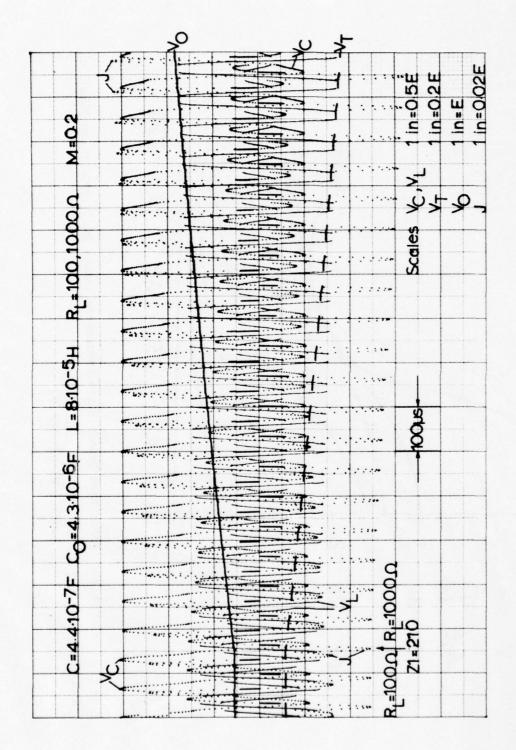


Figure 11. Transient Wave Shapes for Z2=0.875, Step Change of $R_{\rm L}$ from 100-1000 Ω at Z1=210

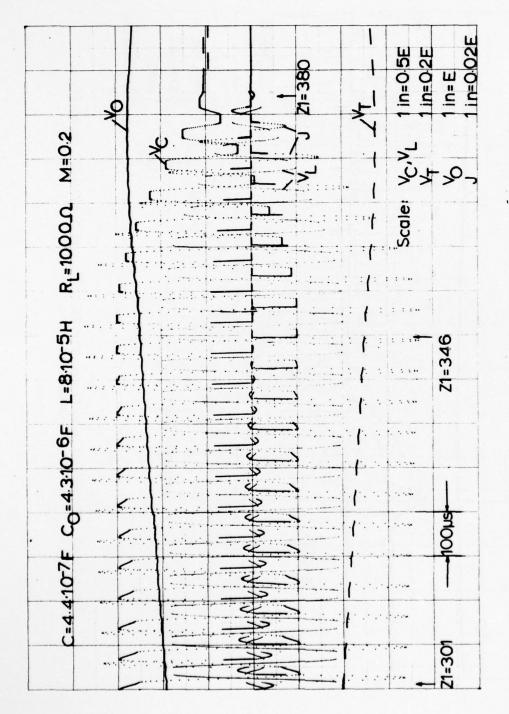


Figure 12. Transfent Wave Shapes for Z2=0.875 and Z1=301-346 (Mode 1), Z1=347-380 (Mode 2)

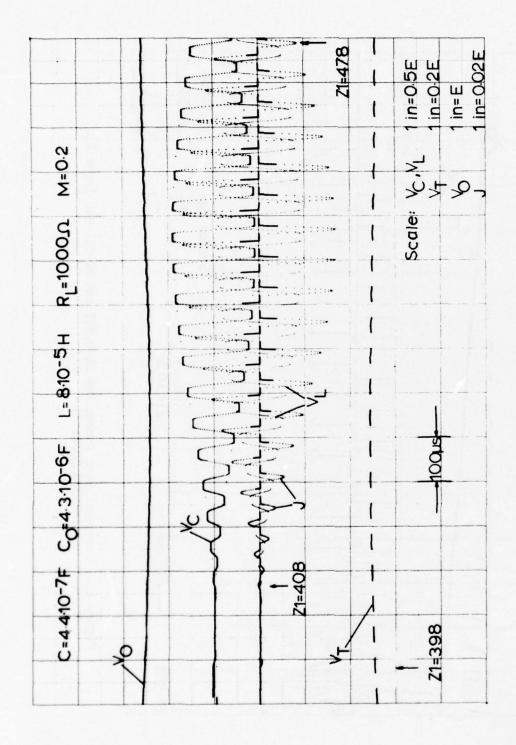


Figure 13. Transient Wave Shapes for Z2=0.875 and Z1=392-397 (Mode 3), Z1=398-478 (Mode 2)

Subsequently, this current increases and slows down the discharge of the output filter capacitor. When the average value of the transistor current again exceeds the load current, the output voltage rises again and the slow oscillation of the system between Mode 2 and Mode 3 may continue. However, the oscillation will be finally damped out as long as $\rm R_L$ is not infinite. The curves in Figure 13 show that for the selected value of Z2 = 0.875 and $\rm R_L$ = 1000 Ω the converter approaches a stable state condition in Mode 2.

CONCLUSIONS

The transient analysis of the series resonance type DC to DC switching converter and the implementation by a computer program have been found to be valuable tools for simulating the complex waveform train in the various switching modes of this converter. The free running feature of this converter is simulated by the restrictions of unipolar current flow in the switching transistors and antiparallel diodes. The only control parameter is the diode conduction time (Z2) which separates the "on state" of the two switching transistors. This leads to 3 operational modes of the converter, distinguished by

- Mode 1 inductor current conduction during both transistor and diode conduction periods;
- Mode 2 inductor current conduction only during transistor conduction period;
- Mode 3 zero inductor current during both transistor and diode conduction periods.

Mode 3 is an intermittent state only but would apply for the border case of an idealized converter (no component losses) under a no load condition, which would be an undefined case with no steady state condition. For finite values of the load resistance, the converter has stable steady state conditions in either Mode 1 or Mode 2 depending on whether a heavy or a light load is applied. The transient Mode 3 appears under a light load condition with an increasing duration as the no load condition is approached.

For each value of diode conduction period 0<22<1, a single set of normalized operational parameters can be shown to exist in the steady state mode. These parameters define the available range of the ratio of input voltage/output voltage, electrical stresses in the power circuit components, and operating switching frequency. Since the average value of the primary voltage on the transformer cannot exceed a value of 0.5E (half the DC-input voltage), in the steady state condition, the converter may be regarded as a buck type switching converter with a limited maximum output/input voltage ratio of 0.5.

The computer program also yields the maximum transient voltage stresses as a function of Z2 and allows determination of the settling time toward steady state conditions.

Transient stresses are shown to be a maximum for Z2=0 and will almost completely subside for Z2=1. Therefore, control of the parameter Z2 can be used effectively to suppress transient stresses for any operational condition except excessive input voltage that would have to be contained by an appropriate input transient suppression circuit. The analysis and computer simulation considers lossless power train components, therefore, it gives no information regarding the operational changes of converter efficiency.

Two considerations for component losses may be made to assess deviations from the ideal case:

- 1. Current independent losses, such as transformer core losses and leakage currents in the output rectifier and filter capacitor, may be regarded as an additional shunt loss to the output load. Therefore, its prime operational influence will be to remove the zero output load instability and present the no load case as a Mode 2 operational condition.
- 2. Current dependent losses like copper losses in the inductor and transformer can be simulated as a lumped resistance in series with the output load. In general, if these losses do not exceed 10% of the power rating of the converter, their influence on the normalized parameters is minor and does not cause significant deviation of the operational mode of the converter as presented in the analysis of the ideal, lossless converter. Therefore, in most design cases, the ideal component-converter analysis will provide a good representation for converter operation.

Power factor losses will increase with the ratio J_m/J_{av} as Z2 increases, but as this ratio changes only by 20% for 0 < Z2 < 1 there is no dramatic effect on efficiency expected over a wide voltage control range.

The computer program is very versatile and permits parametric studies for design optimization by varying either the circuit parameters or the switching control parameter.

RECOMMENDATIONS

The application of the computer program for analysis of control loop design and optimization for the DC/DC switching converter is recommended.

It is further recommended that a study be conducted to determine the advisability of replacing the ideal lumped parameter presentation of power components and switches by more refined component models. A trade-off determination should be made between the increased complexity of the computer program and the necessity for more accurate and realistic results. The latter study will be a necessity when further increases in switching frequencies beyond the 100 kHz range are anticipated.

APPENDIX A

Circuit Analysis

The equivalent circuit, which is derived from the simplified power switching circuit of the series capacitor resonance DC to DC converter, is shown in Figure A-1. It represents a DC input voltage E, a switch S, which can be opened or closed in accordance with the operational switching requirements of the converter, a voltage generator $v_{\rm T}$, which replaces the passive circuit configuration of the output circuit as reflected into the primary of the converter transformer, the resonance inductor L, and the resonance capacitor C. Figure A-2 shows the equivalent circuit for $v_{\rm T}$ on which the restriction:

$$v_T = sign(i) \cdot v_O \cdot M$$
 (A-1)

is imposed.

i transformer primary current

vo . . . DC output voltage

M W1/W2 turns ratio of converter transformer

The following set of simultaneous equations describe the state of the circuit at a particular time instant t.

$$E - v_T - v_L - v_C = 0$$
 (A-2)

$$v_{T} = L \cdot di/dt$$
 (A-3)

$$v_{C} = (1/C) \cdot \int i \cdot dt$$
 (A-4)

$$v_T = sign(i) \cdot v_O \cdot M$$
 (A-5)

$$v_0 = v_0(0) + (1/c_0) \cdot \int_{C_0} \cdot dt$$
 (A-6)

$$i_{C_0} = abs (i/M) - v_0/R_L$$
 (A-7)

Differentiation of (A-6) together with (A-7) yields

$$dv_0/dt = (1/C_0) \cdot [abs (i/M) - v_0/R]$$
 (A-8)

and

$$i = M \cdot C_0 \left[\frac{dv_0}{dt} + v_0/(R_L \cdot C_0) \right] \text{ sign (i)}$$
 (A-9)

Substitution of (A-9) into (A-3) yields:

$$v_{L} = L \cdot M \cdot c_{O} \left[d^{2}v_{O}/dt^{2} + dv_{O}/dt \left(1/R_{L} \cdot c_{O} \right) \right]$$
 (A-10)

Substitution of (A-5) into (A-10) yields:

$$v_{L} = L \cdot c_{O} d^{2}v_{T}/dt^{2} + (L/R_{L}) \cdot dv_{T}/dt$$
 (A-11)

Differentiating (A-4) yields:

$$dv_{C}/dt = i/C (A-12)$$

Integration of (A-3) yields:

$$L \cdot i = \int v_L \cdot dt + v_L(0)$$
 (A-13)

and

$$i = \frac{1}{L} \int v_L dt + i_L(0)$$
 (A-14)

where

$$i_L(0) = v_L(0)/L$$
 (A-15)

Combination of (A-12) + (A-15) yields

$$dv_{C}/dt = \frac{1}{C} \cdot \left[\frac{1}{L} : \int v_{L}dt + i_{L}(0)\right]$$
 (A-16)

and differentiation of (A-16) yields

$$d^2v_c/dt^2 = v_L \cdot 1/(L \cdot c) \tag{A-17}$$

Equations (A-2), (A-11), and (A-17) provide a system of linear differential equations with the circuit voltages v_T , v_L , and v_C as variables. These are chosen as the components of the state variable.

$$V(V_{T}, V_{L}, V_{C})$$
 or $V(V_{1}, V_{2}, V_{3})$

with

$$V_1 = V_T$$
; $V_2 = V_L$; $V_3 = V_C$

The set of second order linear differential equations (A-2), (A-11), and (A-17) transferred into S-space (Laplace transformation) yields the vector equation:

$$V(y) \cdot S(x,y) = F(x) \tag{A-18}$$

where:

S(x,y) state function matrix for S-space

F(x) vector defined by boundary conditions at time=zero

It follows from equations (A-2), (A-11), and (A-17) that:

$$S(x,y) = \begin{pmatrix} 1 & 1 & 1 \\ s^{2} + s/T_{0} & -1/(T_{0} \cdot T_{1}) & 0 \\ 0 & -\omega & s^{2} \end{pmatrix}$$
 (A-19)

with $T_0 = R_L \cdot C_0$; $T_1 = L/R_L$; $\omega^2 = 1/(L \cdot C)$ and:

$$F(x) = \begin{pmatrix} E/S \\ V_1(0)(S + 1/T_0) + V_1'(0) \\ S \cdot V_3(0) + V_3'(0) \end{pmatrix}$$
 (A-20)

where: $V_1(0)$ and $V_3(0)$ initial values of the state function component vectors and $V_1^{(0)}(0)$ and $V_3^{(0)}(0)$ initial values of the derivative of the state function component vectors V_1 and V_3 .

The Eigenvalues or roots of the characteristic equation follow from setting

Determinant S(x,y) = 0 which yields:

$$s^{4} + s^{3}/T_{0} + s^{2}(1/T_{0} \cdot T_{1}) + \omega^{2}) - s \cdot \omega^{2}/T_{0} = 0$$
 (A-21)

Equation (A-21) is of fourth order with one root $S_0 = 0$. The remaining cubic equation

$$s^3 + s^2/T_0 + s(1/(T_0 \cdot T_1) + \omega^2) + \omega^2/T_0 = 0$$
 (A-22)

is characteristic for a comped oscillation with the angular frequency ω and damping constants depending on T_0 and T_1 .

For the oscillatory mode, the other roots (Eigenvalues) of equation (A-22), labeled S_1 , S_2 , S_3 can be written as: S_1 ; $S_2 = S_4 + JS_5$; $S_3 = S_4 - JS_5$.

From equation (A-18) it follows

$$V(y,S) = F(x) \cdot S^{-1}(x,y)$$
 (A-23)

which can be written in the form

$$V(y,s) = \frac{X(0,y)}{s-s_0} + \frac{X(1,y)}{s-s_1} + \frac{X(2,y)\cdot s + X(3,y)}{(s-s_1)^2 + s_5^2}$$
(A-24)

Equation (A-24) yields the general form of the components of the state variable in the time domain as

$$V(y,t) = X(0,y) + X(1,y) \cdot \exp(S_1 \cdot t) + X(2,y) \frac{1}{S_5}$$

$$[(S_4 + X(3,y)/X(2,y))^2 + S_5^2]^{1/2} \cdot \exp(S_4 \cdot t) \cdot$$

$$\sin \cdot (S_5 \cdot t + \alpha)$$
(A-25)

where
$$\alpha = \arctan \cdot (S_5/(S_4 + X(3,y)/X(2,y))$$
 (A-26)

Derivation of Constants X(n,y)

The constants X(n,y) are defined by equations (A-23) and (A-24). Equation (A-24) can be written in the general form:

$$V(y,s) = \frac{A^3(s)}{B^4(s)} \tag{A-27}$$

where $A^3(s)$ is a third order polynom of s and $B^4(s)$ is a fourth order polynom of s with the value $B^4(s) = Det. S(x,y)$ and S_0 , S_1 , S_4 , and S_5 are roots or eigenvalues of S(x,y) (Equation (A-21)).

On the other hand, (A-23) can be written as:

$$V(y,s) = Det. S_{F(x)}(x,y)/Det. S(x,y)$$
 (A-28)

where $S_{F(x)}$ is formed by replacing the y-column of S(x,y) by the column F(x). It follows from (A-27) and (A-28) that

$$A^{3}(s) = Det. S_{F(x)}(x,y)$$
 (A-29)

Since (A-29) must have equal coefficients of s^n on both sides of the equation, it follows from (A-24) and (A-29) that:

$$X(0,y) (s-s_1) [(s-s_4)^2 + s_5^2] + X(1,y) \cdot (s-s_0) [(s-s_4)^2 + s_5^2] + X(2,y) \cdot (s-s_0) (s-s_1) s + X(3,y) (s-s_0) (s-s_1) = Det. S_{F(x)}(x,y)$$
 (A-30)

Applying the aforementioned condition of equal coefficients of s^n to equation (A-30) yield a set of 4 linear equations in X(n,y) as follows:

$$+ X(2,y) + 0 = E_1$$

$$+ X(2,y) \cdot (-s_1 - s_0) + X(3,y) = E_2$$

$$+ X(2,y) \cdot (s_0 \cdot s_1) \div X(3,4) (-s_0 - s_1) = E_3$$

$$+ 0 + X(3,4) \cdot s_0 s_1 = E_4$$

$$(A-31)$$

or in matrix form:

$$X(n,y) \cdot S_n(x,y) = E(n,y) \tag{A-32}$$

where the matrix $S_n(x,y)$ follows from (A-31) as:

$$\mathbf{S}_{\mathbf{n}}(\mathbf{x},\mathbf{y}) = \begin{pmatrix} 1 & 1 & 1 & 0 \\ -(\mathbf{s}_{1} + 2\mathbf{s}_{1}) & -(\mathbf{s}_{0} + 2\mathbf{s}_{1}) & -(\mathbf{s}_{1} + \mathbf{s}_{0}) & 1 \\ \mathbf{s}_{1}^{2} + \mathbf{s}_{5}^{2} + 2\mathbf{s}_{1}\mathbf{s}_{1} & \mathbf{s}_{1}^{2} + \mathbf{s}_{5}^{2} + 2\mathbf{s}_{0}\mathbf{s}_{1} & \mathbf{s}_{0}\mathbf{s}_{1} & -(\mathbf{s}_{0} + \mathbf{s}_{1}) \\ (\mathbf{s}_{1}^{2} + \mathbf{s}_{5}^{2}) \cdot (-\mathbf{s}_{1}) & (\mathbf{s}_{1}^{2} + \mathbf{s}_{5}^{2}) & (-\mathbf{s}_{0}) & 0 & \mathbf{s}_{0}\mathbf{s}_{1} \end{pmatrix}$$

and the matrix E(n,y) is given by the coefficients of s^n for n=3, 2, 1, 0 when Det. $S_{F(x)}$ is evaluated as a polynomial of s^n

$$E(n,y) = \begin{pmatrix} v_1(0) \\ v_1(0)/T_0 + v_3'(0) \\ E/(T_0 \cdot T_1) + & {}^2v_1(0) - v_3(0)/(T_0T_1) \\ v_1(0) \cdot \omega^2/T_0 + \omega^2v_3'(0) - v_3'(0)/(T_0 \cdot T_1) \end{pmatrix}$$

$$E - v_{1}(0) - v_{3}(0)$$

$$E/T_{0} - (v_{1}(0) + v_{3}(0))/T_{0} - v'_{1}(0) - v'_{5}(0)$$

$$-v'_{3}(0)/T_{0}$$

$$0$$

$$v_{3}(0)
 v_{3}(0)/T_{0} + v'_{3}(0)
 \omega^{2} \left[E - v_{1}(0) \right] + v_{3}(0)/(T_{0} \cdot T_{1}) + v'_{3}(0)/T_{0}
 \omega^{2'} \left[E/T_{0} - v_{1}(0)/T_{0} - v'_{1}(0) \right] + v'_{3}(0)/T_{0}T_{1}$$
(A-34)

from equations (A-32), (A-33), and (A-34), it follows

$$X(n,y) = E(n,y) \cdot S_n^{-1}(x,y)$$
 (A-35)

Using equations (A-25), (A-26), and (A-35), the state function V(y,t) is defined in the time domain in terms of circuit parameters which enter into the expressions for $T_0 = R_L C_0$; $T_1 = R_L / L$ and $\boldsymbol{w} = 1/(LC)^{1/2}$ and in terms of initial boundary conditions for the transformer primary voltage $v_1(0)$ and the capacitor voltage $v_3(0)$ and their derivatives $v_1'(0)$ and $v_3'(0)$ which are contained in matrix E(n,y).

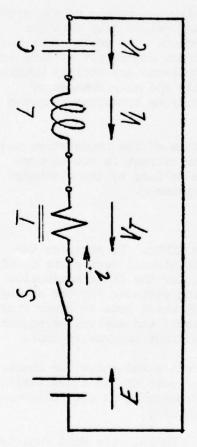


Figure Al. Equivalent Switching Circuit, Primary Loop

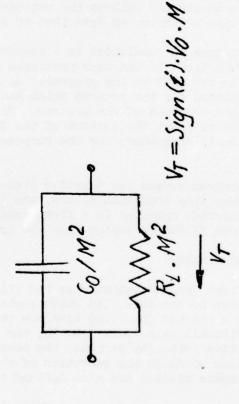


Figure A2. Equivalent Switching Circuit, Secondary Loop

APPENDIX B

Computer Program to Analyze and Plot Waveforms in the Time Domain

INTRODUCTION

The computer program is written in Basic 4 language as implemented on a time-shared system (TSS/8) using a PDP-8/I Minicomputer. The organization of the program closely follows the mathematical modeling analysis of the switching type converter as described in Appendix A.

The program is subdivided in 4 segments, which are stored on the system device (RF-08 Disk) in the user protected area and called into core for operation as required by the program. An independent data record file has been established for the program which handles input and output of data in the 4 chained segments of the program. Small supplementary utility programs were written to print the content of the data file and make changes of certain circuit parameters for the purpose of studying transient response phenomena.

The program senses for negative bias condition of the transistors and diodes. When this condition occurs, the inductor current is set to zero and the converter operates in a first-order mode defined by the discharge of the output filter capacitor into the load resistance.

PROGRAM ORGANIZATION

The first program segment has the file name EKPPO. It provides the initial input to the data file which contains the circuit parameters C, CO, L, Rl, and M and the specified discrete value Z2 for the diode conduction time. Additional parameters like Zl, the counting variable for the string of consecutive switching periods, the constant Z5 which sets an upper limit for the value of Zl in the execution of the program, and scaling parameters for the graphic plotter are also defined in this first program segment.

The major function of segment EKPPO is to define and solve the characteristic equation of the circuit and provide the roots of the characteristic equation as input to the data file for further processing in the follow-on program segments (see line statements 181 through 193).

The second program segment has the file name EKPP1. Its main function is to define the boundary conditions for each of the 4 switching states in terms of either arbitrary initial circuit conditions, or as determined from the state of the circuit at the end of the previous switching state. The matrix elements of the state function equation are calculated and stored in the data file.

The third program segment has the file name LINEQL. This is a subprogram to invert the matrix of the state function and calculate the set of constants to be used with the time domain solutions of the state variables. The fourth and final program segment has the file name EKPP3. In this part of the program, the time dependent values of the state variables are calculated and printed, and/or plotted on a graphic terminal. The values of the state variables at the end of the switching period are stored in the data file for processing of boundary conditions for the subsequent switching period. In case of continuous plotting, this program segment is chained to program segment EKPP1. The program loops through the segments EKPP1, LINEQ1, EKPP3, EKPP1, etc., in a continuous fashion until the specified number of switching periods Z5 is reached. The program also contains statements to limit the transistor and diode switching periods whenever the primary loop current reaches zero, thereby modeling the conditions for unipolar conduction of transistors and diodes. Thus, the conduction time is independent of the specified range of the time variable which does not exceed the half period time of the resonant frequency but it can be much shorter in the case of specific operational modes of the converter.

Two utility programs have been written which provide for checking and new input to the data file, independent of the program execution.

Program segment "EKD1" prints the content of the data file as output on the teletype. Program segment "EKD2" is used to change the input parameters of the circuit (C, CO, L, Rl, and M) and the initial boundary conditions and plotting range, as defined by data lines numbers 61 through 68.

If the program is halted in any switching period, the combined use of EKD1 and EKD2 can facilitate checking of boundary relations and input of step functions for the purpose of studying transient behavior.

COMMENTS

A final note on the usefulness of this computer modeling program is in order. Safeguards have been provided to abort the program if circuit parameters are selected which do not meet the criteria for resonance oscillation in the primary circuit.

In program segment "EKPPO" there is a printout of the critical load resistance R2. A value R1 < R2 would provide overdamping without oscillations and an abortion of the program. On the other hand, a value R1 >>> R2 will cause long transient periods when operational parameters are changed and in some specific cases will result in modes during which either the diode or the transistor current or both are zero during a number of consecutive switching periods.

A study of these conditions is of particular interest with respect to stability problems of the circuit but is beyond the scope of this report.

Although the program has been written for a constant value of Z2, the program can be interrupted at any time to change the value of Z2 and to continue the study of transient behavior with this new value of Z2. Ultimately, Z2 could be made subject to restriction of output parameters (output voltage, output current) or limitation of stresses in electrode components ($V_{\rm Cpp}$) to implement desired control functions with automatic feedback.

LISTING OF PROGRAM SEGMENTS

The following is a list of symbols used in the various program segments:

A(0,0) to A(3,3)	Matrix elements of state function matrix
B(0) to B(23)	Matrix elements of sub-matrices of state function matrix
C	Equivalent resonance capacitance (C = Cl + C2)
co	Output filter capacitance
D (in EKPPO)	Criterion for solution of characteristic equation
DO	Criterion for zero current approach
D4(I)	Array variable (I = 0 to 20)
D4(0)	Variable to store capacitor voltage $V_0(1)$
D4(1)	Variable to store inductor voltage $V_{O}(0)$
D4(2)	Variable to store inductor current $J_0(1)$
D4(3)	Dummy variable (not used)
D4(4)	Variable to store elapsed time (T2)
D4(5)	Variable to store capacitor voltage $V_{\bigcirc}(1)$
D4(6)	Variable to store inductor current $J_0(1)$
D4(7)	Variable to store inductor voltage $V_0(0)$
D4(8) thru D4(20)	Dummy variables (not used)
D5(I)	Array variable (I = 0 to 7)
D5(0)	Variable to store state function subscript Y
D5(1)	Variable to store elapsed switching time Nl
D 5(2)	Variable to store capacitor voltage $V_{0}(1)$
D5(3)	Variable to store inductor current $J_0(1)$
D5(4)	Variable to store transformer voltage $V_0(2)$
D5(5)	Variable to store switch count variable Z1
D5(6)	Variable to store capacitor voltage $V_{O}(1)$
D5(7)	Variable to store inductor current $J_0(1)$

E(I)	Array variable (I = 0 to 3)
E(0)	Initial value of capacitor voltage $V_0(1)$
E(1)	First derivative of capacitor voltage at time zero
E(2)	Initial value of transformer voltage $V_0(2)$
E(3)	First derivative of transformer voltage at time zero
F(I)	Array variable (I = 0 to 3)
F(0)	
F(1)	Variables defining switch boundary conditions
F(2)	variables defining switch boundary conditions
F(3)	
G(I)	Array variable (I = 0 to 4)
G(0)	Storage variable for capacitance value C
G(1)	Storage variable for capacitance value C
G(2)	Storage variable for inductance value L
G(3)	Storage variable for load resistance RL
G(4)	Storage variable for transformer winding ratio M
H(I)	Array variable (I = 0 to 6)
H(O)	Storage variable for root S ₁ of characteristic equation
H(1)	Storage variable for root S2 of characteristic equation
H(2)	Storage variable for root S3 of characteristic equation
н(3)	Storage variable for operating frequency
H(4)	Storage variable for time constant $T_0 = R_L \cdot C_0$
H(5)	Storage variable for time constant $T_1 = R_L/L$
н(6)	Storage variable for angular frequency W4 = 1/VL·C
I	Integer variable used in array statements
J	Integer variable used in array statements
JO(1)	Variable describing inductor current normalized value

K(I)	Array variable (I = 0 to 3)
K(0)	Stores progressing elapsed time of each switching period (N1)
K(1)	Specifies number of switching periods Z5
K(2)	Full scale value of time for graphic plot
K(3)	Stores normalized diode conduction time Z2
L	Value of inductance in series-resonant circuit
L(I)	Dummary array variable (not used) (I = 0 to 4)
м	Value of transformer winding ratio W1/W2
NI	Value of switching period time
N2	Time increment
P	Parameter in cubic equation
Q	Parameter in cubic equation
ðī	Parameter in cubic equation
92	Parameter in cubic equation
Q3	Parameter in cubic equation
Q ¹ 4	Parameter in cubic equation
RL	Value of load resistance R_L
R2	Value of critical load resistance
SI	Root of characteristic equation
S2	Root of characteristic equation (real part)
s 3	Root of characteristic equation (imaginary part)
то	Time constant (TO = $R_L \cdot CO$)
Tl	Time constant (T1 = R_L/L)
T2	Time variable (within switching period)
T 5	Total elapsed time (at end of switching period)
т6	Full scale value of time for graphic plot

T 7	Upper limit value of time for graphic plot
T(3,3)	Array variable (matrix $T(3,3)$ = Matrix $A^{-1}(3,3)$
VO(I)	Array variable (I = 0 to 3)
vo(o)	Variable inductor voltage
VO(1)	Variable capacitor voltage
Vo(2)	Variable transformer voltage
vo(3)	Variable output voltage
W3	Effective angular frequency
W14	Resonance angular frequency
X\$(I)	String variable (I = 0 to 3)
X(I)	Array variable (I = 0 to 3)
X (0)	Constant in time dependent solutions of VO
X(1)	Constant in time dependent solutions of VO
X(5)	Constant in time dependent solutions of VO
X (3)	Constant in time dependent solutions of VO
Y	Index of state function variable
Yl	Switch mode index
X5	Switch mode index
z	Argument for Sin and Cos functions
Zl	Counting variable for switch periods
Z 5	Number of switch periods(Z1) specified for plotting

PROGRAM SEGMENT "EKPPO"

```
.k FASIC4
NEW ON OLD -- OLD
OLD FROCKAN NAME -- EKFPO
 EADY
LIST
   4 KECOKD G(4), H(6), D5(7), K(4)
   6 OPEN 8,"DATAI"
   8 LET J=0
  31 FRINT
  40 INPUT C.CO.L.KI.N
  41 LET G(A)=CYLET G(1)=CAYLET G(2)=1 YLET G(3)=KIYLET G(4)=N
  45 LET TP=N+2*R1*(CM/N+2)
  46 LET TI=L/(N+2*K1)
  50 PRINT "10=";10;"11=";11
  55 LET 13=1/(SCK(L *C*(CM/N 12)/(CP/N 12+C)))
  60 LET M4=1/SCR(L+C)
  61 FRINT "k3="k3;"k4=";k4
  65 PHINT
  66 PRINT "REDUCED CUPIC ECUATION S+3+F+S+L=F "
  70 LET P=(1312)-1/(3+1012)
75 LET (=(2+9*(1012)*(3*(k4+2)-(k3+2)))/(3*10)*3
  85 LET D=(F/3)+3+(C/2)+2
  87 LET K2=1/( 4+C0+SCK(3))
  88 PHINT "R2=";R2
  90 IF SCN(D) <=0 THEN 100
 95 GOTO 110
100 PRINT "RESULT OVERDAMPED OSCILLATION CHANGE CINCUIT FARAMETERS"
 102 INPUT C.CO.L.RI.N
 105 6010 45
 110 FRINT "OSCILLATORY CASE"
 111 PRINT
 125 LET 03=-0/2+SCK(D)
 126 LET 04=-0/2-SCR(D)
 127 IF 63 O THEN 129
 128 COTO 133
 129 LET 61=(-63)*(1/3)
130 LET C1=-61
 132 0010 134
 133 LET 61=63+(1/3)
134 IF 64<0 THEN 136
 135 6010 149
 136 LET (2=(-(4)+(1/3)
 137 LET 62=-C2
 139 6010 165
 140 LET 02=64*(1/3)
165 LET SI=(C1+(2)-1/(3+10)
 170 LET S2=-S1/2-1/(2+10)
 171 LET S3=SCR(3)*(61-62)/2
 180 PRINT
 181 PRINT "KESULT"
181 PRINT "THE KOOTS OF THE CHARACTERISTIC EQUATION ARE: "
183 PRINT "REAL ROOT SI= ";S]
184 PRINT "COMPLEX ROOT $2+J*53=";S2;"+J*";S3
185 PRINT "COMPLEX ROOT $2-J*53=";S2;"-J*";S3
 188 LET F#=53/(2+3-141593)
 190 PRINT "OPERATING FREQUENCY FP="153/(2+3.141593);"HERTZ"
 192 LET H(0)=SINLET H(1)=S2NLET H(2)=S3NLET H(3)=F0
193 LET H(4)=T0NLET H(5)=TINLET H(6)=W4
 194 LET D5(0)=01LET D5(5)=01K(P)=01K(1)=01K(2)=01K(3)=0
 195 PRINT "NUMBER OF SWITCHING PERIODS TO PLOT 75="ININFUT 75
 196 K(1)=75
 197 17=75+3.141593/HC23NFKINT "17="117
 198 PRINT "FULL SCALE VALUE OF TIPE AXIS T6="JNINFUT T6NK(2)=16
199 PRINT "DIODE CONDUCTION PENIOD 72="JNINFUT Z2NK(3)=22
200 LET 1=0
202 PUT 8,4,1
216 CHAIN "EKPFI".
250 END
```

PROGRAM SEGMENT "EKPP1"

```
BEST AVAILABLE COPY
OLD PHOGHAM NAME -- EMPPI
              50 RECORD C(4).H(6).D5(7).K(4)
60 OPEN R."DATAI"
70 LET I=0
     70 LET 1=0

H0 CET 8,50,1

R7 LET S1=H(0)NLET S2=H(1)NLET S3=H(2)NLET W0=H(3)NLET 10=H(4)

R8 LET T1=H(5)NLET W4=H(6)NLET 72=K(3)

130 RECOND A(3,3),F(3),L(4)

130 DIN X1(3),E(3)

137 FOR I=0 TO 3

138 READ X5(1)
     13P FEAD X5(1)
14N NEXT I
141 Y=75(0) \ 1F Y>0 THEN 143
142 PHINT "INITIAL ROUNDARY CONDITIONS AT TIME = 0 "
143 71=75(5)\IF 71=0 THEN 145
144 0710 146
145 IF Y=0 THEN 162
146 73=71-4*INT(71/4)\Y!=(-1)*INT(73)\Y2=(-1)*INT(73/2)
     146 73=71-4*|NT(71/4)\Y|=(-1)*|NT(2)
147 |F Y|=1 THEN149
148 |F Y|=-1 THEN 152
149 |F Y2=1 THEN 154
150 |F Y2=-1 THEN 154
151 PKINT " INPUT EKKOK " \(COTO 144
152 |F Y2=-1 THEN 159
153 |F Y2=1 THEN 159
  154 IF 72=0 THEN 260
155 E(0)=1-D5(6)\\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}{2}\)\(\frac{1}\)\(\frac{1}{2}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\(\frac{1}\)\
        155 E(#)=1-D5(6)\F(1)=-D5(7)/G(#)\E(2)=-D5(4)
     190 LET F(3)=L442*E(2)/T0*L42*E(3)-E(1)/(10*T1)
191 G010 199
192 LET F(0)=1-E(0)-E(2)\LET F(1)=(1-E(0)-E(2))/10-E(1)-E(3)
193 LET F(2)=-E(1)/T0\LET F(3)=0
194 G010 199
195 LET F(0)=E(0)\LET F(1)=E(0)/T0*E(1)
196 LET F(2)=L442*E(1-E(2))*E(0)/(T0*T1)*E(1)/T0
197 LET F(3)=L442*E(1/T0*LE(3)-E(2)/T0)*E(1)/(10*T1)
199 DATA "X(0)","X(1)","X(2)","X(3)"
  197 LEI F (3)=k412*(1710-E(3)-E(2)710)*E(1)7(10*II)

199 DATA "X(0)","X(1)","X(2)","X(3)"

215 LET I = 1

229 FUT 8,130,1

235 LET I = 0

240 PUT 8,50,1

250 CHAIN "LINEUT"

261 F Y2=1 THEN 270

262 E(0)=1-D5(2)XE(1)=N\(2)=D5(4)

263 E(0)=1-D5(2)XE(1)=N\(2)=D5(4)

264 E(0)=1-D5(2)XE(1)=N\(2)=D5(4)

265 F(NIT "POUNDARY CONDITIONS FOR TR-2 CONDUCTION PERIOD"

266 FRINT "71="171

269 FRINT "E(0)="JE(0),"E(1)="JE(1),"E(2)="JE(2),"E(3)="JE(3)\GOTO 170

270 E(0)=1-D5(6)XE(1)=N\(2)=D5(4)

272 E(3)=-AFS(E(2))/H(4) \ IF Y>0 THEN 170

273 FRINT "POUNDARY CONDITIONS FOR TR-1 CONDUCTION PERIOD"

274 FRINT "71="171

275 PRINT "E(0)="JE(0),"E(1)="JE(1),"E(2)="JE(2),"E(3)="JE(3)\GOTO 170

370 END
```

PROGRAM SEGMENT "LINEQL"

```
OLD
OLD PROGRAM NAME -- LINEUI
READY
LIST
 100 REM PROGRAM TO SOLVE 4-LINEAR EGUATIONS
 110 RECORD A(3,3),F(3),L(4)
120 RECORD X(3),D4(20)
 122 OPEN 8,"DATA1"
 125 LET I=1
 130 GET 8,110,1
 135 1=2
 140 GET 8,120,1
 180 DIN P(23),T(3,3)
 198 LET E(0)=A(2,2)+A(3,3)-A(2,3)+A(3,2)
 191 LET P(1)=A(1,2)+A(3,3)-A(1,3)+A(3,2)
 192 LET B(2)=A(1,2)+A(2,3)-A(2,2)+A(1,3)
 193 LET P(3)=A(2,1)+A(3,3)-A(2,3)+A(3,1)
 194 LET F(4)=A(1,1)*A(3,3)-A(1,3)*A(3,1)
 195 LET P(5)=A(1,1)+A(2,3)-A(1,3)+A(2,1)
 196 LET B(6)=A(2,1)*A(3,2)-A(3,1)*A(2,2)
 197 LET F(7)=A(1,1)*A(3,2)-A(3,1)*A(1,2)
 198 LET E(8)=A(1,1)+A(2,2)-A(2,1)+A(1,2)
 199 LET P(9)=A(0,2)+A(3,3)-A(0,3)+A(3,2)
 200 LET F()0)=A(0,2)*A(2,3)-A(0,3)*A(2,2)
201 LET F(11)=A(0,1)*A(3,3)-A(0,3)*A(3,1)
 202 LET B(12)=A(0,1)+A(3,2)-A(0,2)+A(3,1)
 203 LET F(13)=A(0,2)+A(1,3)-A(0,3)+A(1,2)
 204 LET F(14)=A(0,1)*A(2,3)-A(0,3)*A(2,1)
 205 LET P(15)=A(0,1)+A(2,2)-A(0,2)+A(2,1)
 206 LET F(16)=A(P,1)+A(1,3)-A(P,3)+A(1,1)
 207 LET P(17)=A(0,1)+A(1,2)-A(0,2)+A(1,1)
 208 LET B(18)=A(0,0)+A(1,1)-A(1,0)+A(0,1)
 209 LET B(19)=A(2,0)*A(0,1)-A(0,0)*A(2,1)
 210 LET P(20)=A(0,0)+A(3,1)-A(3,0)+A(0,1)
 211 LET B(21)=A(1,0)+A(2,1)-A(2,0)+A(1,1)
 212 LET B(22)=A(3,0)+A(1,1)-A(1,0)+A(3,1)
 213 LET B(23)=A(2,0)+A(3,1)-A(3,0)+A(2,1)
 214 PKINT
 215 LET D=P(P)+B(18)+B(1)+B(19)+B(2)+B(20)+B(9)+B(21)+B(10)+B(22)
 216 LET D=D+P(13)+P(23)
 220 LET T(0,0)=(A(1,1)*P(0)-A(2,1)*P(1)+A(3,1)*F(2))/D
 221 LET T(1,0)=(-A(1,0)*B(0)+A(2,0)*B(1)-A(3,0)*B(2))/D
222 LET T(2,0)=(A(1,0)*B(3)-A(2,0)*B(4)*A(3,0)*B(5))/D
 223 LET T(3,0)=(-A(1,0)+P(6)+A(2,0)+F(7)+-A(3,0)+F(8))/D
 225 LET T(0,1)=(-A(0,1)+B(0)+A(2,1)+F(9)-A(3,1)+E(10))/D
226 LET T(1,1)=(A(0,0)*B(0)-A(2,0)*F(9)+A(3,0)*B(10))/D
227 LET T(2,1)=(-A(0,0)*F(3)+A(2,0)*F(11)-A(3,0)*B(14))/D
 228 LET T(3,1)=(A(0,0)+P(6)-A(2,0)+F(12)+A(3,0)+F(15))/D
 230 LET T(0,2)=(A(0,1)+B(1)-A(1,1)+F(9)+A(3,1)+B(13))/D
231 LET T(1,2)=(-A(0,0)*P(1)+A(1,0)*F(9)-A(3,0)*F(13))/D
232 LET T(2,2)=(A(0,0)*P(4)-A(1,0)*F(11)+A(3,0)*R(16))/D
 234 LET T(3,2)=(-A(0,0)+F(7)+A(1,0)+F(12)-A(3,0)+B(17))/D
 236 LET T(0,3)=(-A(0,1)+P(2)+A(1,1)+P(10)-A(2,1)+P(13))/D
 237 LET T(1,3)=(A(0,0)+B(2)-A(1,0)+F(10)+A(2,0)+B(13))/D
 238 LET T(2,3)=(-A(0,0)+P(5)+A(1,0)+P(14)-A(2,0)+B(16))/D
 239 LET 1(3,3)=(A(0,0)+B(8)-A(1,0)+P(15)+A(2,0)+P(17))/D
 250 LET X(0)=T(0,0)+F(0)+T(0,1)+F(1)+T(0,2)+F(2)+T(0,3)+F(3)
 252 LET X(1)=T(1,0)*F(0)+T(1,1)*F(1)+T(1,2)*F(2)+T(1,3)*F(3)
254 LET X(2)=T(2,0)+F(0)+T(2,1)+F(1)+T(2,2)+F(2)+T(2,3)+F(3)
256 LET X(3)=1(3,0)*F(0)+T(3,1)*F(1)*T(3,2)*F(2)+T(3,3)*F(3)
257 PRINT
 280 LET 1=2
290 PUT 8,120,1
292 IF D4(10)=0 THEN 295
         D4(10)=1 THEN 296
293 IF
 294 PHINT "SPECIFY DACIAL FOR CHAIN STATEMENT" FRINTIGOTO 300
295 CHAIN "EKPP3"
296 CHAIN "EKPP 4"
```

PROGRAM SEGMENT "EKPP3"

```
OLD
OLD PROCRAM NAME -- EKPP2-3
READY
LIST
   25 OPEN 8."DATA1"
   30 RECORD G(4),H(6),D5(7),K(4)
   32 KECOHD X(3), D4(20)
   34 LET 1=0
36 GET 8.30.1
   38 LET 1=2
40 GET 8,32,1
50 PKINT "D4(2)=";D4(2),"D4(6)=";D4(6)
150 T5=K(0)\75=K(1)\T6=K(2)\72=K(3)
152 Y=D5(0)\PRINT "Y=";YPRINT " T5=";T5\PKINT
154 71=D5(5)\PKINT "71=";Z1
159 73=71-4*INT(71/4)\Y1=(-1)*INT(Z3)\Y2=(-1)*INT(Z3/2)
160 IF Y1=1 THEN 162
161 IF Y1=1 THEN 164
162 IF Y2=1 THEN 166
163 IF Y2=-1 THEN 166
164 IF Y2=-1 THEN 169
165 IF Y2=-1 THEN 168
166 PRINT "TRANSISTOR 1 CONDUCTION PERIOD"\GOTO 171
167 PKINT "TKANSISTOR 2 CONDUCTION PERIOD"\GOTO 171
168 PKINT "DIODE 1 CONDUCTION PERIOD"\GOTO 170
169 PKINT "DIODE 2 CONDUCTION PERIOD"\GOTO 170
170 GOTO 172
  176 6010 172
  171 72=1
 172 K=SER((H(1)+X(3)/X(2))+2+H(2)+2)+SGN(H(1)+X(3)/X(2))
 173 N1=72+3.141593/H(2)\N2=N1/25\DIM VA(3), JA(1)
 174 IF Y=0 THEN 175\GOTO 438
175 D0=AES(2*N2*G(0)*H(2)*2*X(2))\PRINT "D0="JD0\FKINT "NI="JNI
 178 PHINT "PLTP" YPKINT
 IRM FOR 12=M TO NI STEF N2
IRS LET 7=H(2)+T2+ATN(H(2)/(H(1)+X(3)/X(2)))
 190 LET V0(1)=X(0)+X(1)+EXP(H(0)+T2)+X(2)+EXP(H(1)+T2)+K+SIN(Z)/H(2)
  195 LET J0(1)=G(0)+(X(1)+H(0)+EXP(H(0)+T2))
 196 LET JR(1)=JR(1)+G(R)+(H(1)+X(2)+EXP(H(1)+T2)+K+SIN(Z)/H(2))
 197 LET JR(1)=JR(1)+G(R)+(H(2)+X(2)+EXF(H(1)+T2)+K+COS(Z)/H(2))
 198 IF T2 <= 3+N2 THEN 260
199 IF AFS(JØ(1)) <= DØ THEN 205
 200 6010 260
 205 LET NI=T2\FRINT "NI="JNI\FRINT
210 IF YI=-1 THEN 220
211 IF J0(1)<0 THEN 213
212 D4(5)=V0(1)\D4(6)=J0(1)\G0T0 237
 213 J0(1)=0\V0(1)=D4(5)\D4(6)=J0(1)
 215 0010 237
 220 IF JO(1)>0 THEN 225
 222 D4(4)=12\D4(P)=VP(1)\D4(2)=JP(1)\COTO 237
225 JP(1)=P\VP(1)=D4(P)\D4(2)=JP(1)
 225 Jr(1)=evvn(1)=B4(0)\D4(2)=Jn(1)
237 JF Y2=1 THEN 240
239 Vn(1)=1-Vn(1)\Jn(1)=-Jn(1)
240 PRINT INT(9999*(15+T2)'T6),INT(5000+4999*Vn(1)/2.5)
242 PRINT INT(9999*(15+T2)/T6)," ";
 245 PRINT INT (5000+4999+J0(1)/0.1)\PKINT
 250 GOTO 300
 260 IF YI=-1 THEN 265
261 IF JM(1)<0 THEN 268
264 D4(5)=VM(1)\D4(6)=JM(1)\GOTO 270
 265 IF JA(1)>0 THEN 267
266 P4(4)=T2\D4(0)=V4(1)\D4(2)=J4(1)\C0TO 278
267 J4(1)=0\V4(1)=D4(0)\D4(2)=J4(1)\C0TO 278
 268 J0(1)=0\V0(1)=D4(5)\D4(6)=J0(1)\GOTO 270
 270 IF Y2=1 THEN 280
275 VA(1)=1-VA(1)\JA(1)=-JA(1)
 280 FRINT INT(9999*(T5+T2)/T6),INT(5000+4999*V0(1)/2.5)
285 PRINT INT(9999*(T5+T2)/T6),"
286 PRINT INT(5000+4999*J0(1)/0.1)\PRINT
 300 PRINTYPRINT "PLITTYPRINT
```

```
305 LET DE=D0/20
306 PRINT "D4(2)=";D4(2),"D4(6)=";D4(6)
307 IF 72<1 THEN 396
308 PRINTYFRINT "FLIP"YPRINT
310 FOR T2=N1 TO 1.10*N1 STEP N2/20
315 LET 7=H(2)*T2+ATN(H(2)/(H(1)+X(3)/X(2)))
320 LET V0(1)=X(0)*X(1)*EXF(H(0)*T2)+X(2)*EXF(H(1)*T2)*K*SIN(2)/H(2)
330 LET J0(1)=G(0)*(X(1)*H(0)*EXP(H(0)*T2))
340 LET J0(1)=J0(1)+G(0)*(H(1)*X(2)*EXP(H(1)*T2)*K*SIN(Z)/H(2))
350 LET J0(1)=J0(1)+G(0)+(H(2)+X(2)+EXP(H(1)+T2)+K+COS(Z)/H(2))
362 IF APS(JP(1)) <= DO THEN 364
363 GOTO 380
364 IF Y1=-1 THEN 366
365 IF D4(6)=0 THEN 370\D4(5)=V0(1)\QQTO 372
366 IF D4(2)=0 THEN 368
367 D4(4)=12\D4(8)=V8(1)\G010 372
379 LET NI=T2\FRINT\FRINT "NI=";NI\FRINT\GOTO 396
380 IF Y1=-1 THEN 383
381 IF D4(6)=0 THEN 385
382 D4(5)=V0(1)\GOTO 386
383 IF D4(2)=M THEN 384\D4(4)=12\D4(0)=VM(1)\G010 386
384 JM(1)=A\VM(1)=D4(0)\D4(2)=JM(1)\G010 386
385 J0(1)=0\V0(1)=D4(5)\D4(6)=J0(1)
386 IF Y2=1 THEN 390
388 V0(1)=1-V0(1)\J0(1)=-J0(1)
390 PRINT INT(9999*(15+T2)/T6),INT(5000+4999*V0(1)/2-5)
392 PRINT INT(9999*(15+T2)/T6),"
394 PRINT INT(5000+4999*J0(1)/0-1)\PRINT
 395 NEXT TE
396 72=×(3)
398 PRINTYPRINT "PLIT"YPRINTYIF 72=0 THEN 425
398 PRINTYPHINI THE TOPRINTY 22-9 THEN 425

400 IF Y2=1 THEN 422

405 IF Y1=1 THEN 420

415 D5(6)=V0(1)\D5(7)=J0(1)\D5(1)=N1 \ GOTO 429

420 D5(2)=V0(1)\D5(3)=J0(1)\D5(1)=N1 \ GOTO 429
422 IF Y1=1 THEN 424
423 D5(6)=1-V0(1)\D5(7)=-J0(1)\D5(1)=N1 \ G0T0 429
424 D5(2)=1-V0(1)\D5(3)=-J0(1)\D5(1)=N1 \ G0T0 429
425 IF Y2=-1 THEN 427
426 D5(2)=\P(1)\D5(1)=N1\G0T0 429
427 D5(6)=1-\P(1)\D5(1)=N1\C0T0 429
 429 Y=Y+1\D5(0)=Y\FRINT "D5(1)=";D5(1)\PKINT
430 LET 1=0
432 PUT 8,30,1
433 I=2
434 PUT 8,32,1
435 GOTO 495
438 72=x(3)
439 PRINT "D4(2)=";D4(2),"D4(6)=";D4(6)
439 FRINT "D4(2)="JD4(2),"D4(6)="JD4(6)
440 LET N|=D5(1)\LET N2=N|/25\FRINT "N|="JN\FKINT\IF Y=1 THEN 472
445 IF Y = 2 THEN 452
446 FRINT "ERROK IN ASIGNMENT OF Y " \ GOTO 600
452 FRINT\FRINT "PLTP"\PRINT
453 FRINT\FRINT "7 DEGREE";" TRANSF. VOLTAGE"," OUTPUT VOLTAGE"
455 FOR T2= 0 TO N|*1.005 STEP N2
456 LET 7=H(2)*T2*ATN(H(2)/(H(1)*X(3)/X(2)))
457 LET V0(2)=X(0)*X(1)*EXP(H(0)*T2)*X(2)*EXP(H(1)*T2)*K*SIN(7)/H(2)
458 LET V0(3)=AFS(V0(2))/G(4)\IF Y1=-1 THEN 460
459 J0(1)=D4(6)\IF J(1)=E THEN 460
459 JP(1)=D4(6)\IF JP(1)=E THEN 462\D4(8)=VP(2)\G0T0 463 460 JP(1)=D4(2)\IF JP(1)=P THEN 462
461 D4(3)=VP(2)\GOTO 463
462 V0(2)=-D5(4)*EXF(-(T2-D4(4))/H(4))\V0(3)=ABS(V0(2))/G(4)
463 IF Y2=1 THEN 465
465 PRINT INT(9999*(15+12)/16), INT(5000+4999*V0(2)/1.0)
466 PRINT INT(9999*(15+12)/16)," ", INT(5000+4999*V0(3)/5)\PRINT
468 NEXT T21 GOTO 484
472 PRINTYPRINT "PLTL" YPRINT
```

```
473 PRINT "Z-DEGREES", "INDUCTOR VOLTAGE" FOR T2=0 TO NI+1.005 STEP N2
474 LET 7=H(2)*T2+ATN(H(2)/(H(1)+X(3)/X(2)))
475 LET VO(0)=X(0)+X(1)+EXP(H(0)+T2)+X(2)+EXP(H(1)+T2)+K+SIN(7)/H(2)
476 IF Y1=-1 THEN 478
477 J0(1)=D4(6)\1F J0(1)=0 THEN 510\D4(7)=V0(0)\G0T0 480
478 J0(1)=D4(2)\1F J0(1)=0 THEN 479\D4(1)=V0(0)\G0T0 480
479 VO(0)=0\D4(1)=0
489 IF Y2=1 THEN 482
481 VA(A)=-VA(A)
482 PRINT INT(9999*(T5+T2)/T6), INT(5000+4999*VA(0)/2.5)\PKIN1
483 NEXT T2\Y=Y+1\D5(0)=Y\GOTO 490
484 IF Y2=1 THEN 486
485 VA(2) =- VA(2)
486 D5(4)=V0(2)\Y=0\D5(0)=Y \ 1F 72=0 THEN 488
487 71=71+1\GOTO 489
488 71=71+2
489 D5(5)=71\T5=T5+D5(1)\K(0)=T5\JF 71>75 THEN 496
490 PRINTYPRINT "PLTT" \1=0\PUT 8,30,1
492 LET 1=2
493 PUT 8,32,1
494 IF 71+2>75 THEN 520
495 CHAIN "EMPPI"
496 I=2
497 PUT 8,32,1
498 I=0\PUT 8,30,1
499 GOTO 600
510 VO(0)=0\D4(7)=0\GOTO 480
520 D4(10)=0\GOTO 495
600 PRINT "FLTT" NEND
```

PROGRAM SEGMENT "EKDL"

OLD OLD PROGRAM NAME -- EKDI READY LIST 50 PRINT "PROGRAM TO PRINT CONTENT OF DATA! ! " 60 PRINT 70 PRINT 100 RECORD G(4),H(6),D5(7),K(4) 200 RECORD A(3,3),F(3),L(4) 300 RECORD X(3), D4(20) 400 OPEN 8."DATA1" 420 LET I=0 430 GET 8,100,1 440 LET I=1 450 GET 8,200,1 460 LET 1=2 470 GET 8,300,I 500 FOR I=0 TO 4 510 PRINT "G(";1;")=";G(1), 512 NEXT I NPRINT 515 PRINT 520 FOR I=0 TO 6 530 PRINT "H(";1;")=";H(1), 532 NEXT I VPRINT 535 PRINT 540 FOR I=0 TO 7 550 PRINT "D5("; I;")="; D5(1), 551 NEXT INPRINTAPRINT 552 FOR I=0 TO 4 553 PRINT "K(") [;")=";K([), 554 NEXT I \PRINT\PRINT 555 PRINT "MATRIX A(3;3)" 560 FOR 1=0 TO 3 565 FOR J=0 TO 3 566 PRINT A(I,J), 567 NEXT JAPRINT " " 568 NEXT I YPRINT 569 PRINT 570 FOR I=0 TO 3 575 PRINT "F("; I;")=";F(I), 576 NEXT I NPRINTNPRINT 577 FOR I=0 TO 4 578 PRINT "L("; [;")=";L([), 579 NEXT I \PRINT\PRINT 580 FOR I=0 TO 3 585 PRINT "X(";1;")=";X(1), 586 NEXT I YPRINT 588 PRINT 590 FOR I=0 TO 20 595 PRINT "D4(";1;")=";D4(1), 596 NEXT I YPRINT

597 IF D4(10)=1 THEN 599

598 GOTO 600 599 CHAIN "EKD2"

600 END

PROGRAM SEGMENT "EKD2"

OLD

OLD PROGRAM NAME -- EKD2

READY

LIST

- 40 PRINT "DATA RECORD CHANGE"
- 50 RECORD G(4),H(6),D5(7),K(4)
- 55 RECORD X(3), D4(20)
- 60 OPEN 8,"DATA1"
- 61 FOR I=0 TO 4\INPUT G(I)\NEXT I
- 62 FOR I=0 TO 6\INPUT H(I)\NEXT I
- 63 FOR I=0 TO 7 \ INPUT D5(I)\NEXT I
- 64 FOR I=0 TO 4 \ INPUT K(I) \ NEXT 1
- 65 FOR I=0 TO 3 \ INPUT X(I) \ NEXT I
- 66 FOR I=0 TO 6 \ INPUT D4(1) \ NEXT I
- 67 FOR I=7 TO 13 \ INPUT D4(I) \ NEXT I
- 68 FOR I= 14 TO 20 \ INPUT D4(I) \ NEXT I
- 70 I=0 \ PUT 8,50,1
- 80 I=2 \PUT 8,55,1
- 85 IF (D5(5)+20)=K(1) THEN 95
- 90 GOTO 100
- 95 CHAIN "EKPP1"
- 100 END